REMARKS

Applicants are submitting a supplemental IDS herewith, which includes a copy of a PCT International Search Report and Written Opinion (hereinafter "Opinion"). In this Opinion, the European examiner identified FIG. 30 at page 23 of Document D1 (IDT "3.3 Volt CMOS SyncFIFO IDT72V205" datasheet) as showing a depth expansion configuration of FIFOs. Applicants acknowledge that FIG. 30 shows a depth expansion configuration using multiple FIFO memories, however, this configuration is achieved using a daisy chain technique. This daisy chain technique involves using a plurality of FIFO memories connected to a common data input port (DATA IN) and a common data output port (DATA OUT). In stark contrast, the subject matter of Claim 7 is directed to a cascaded arrangement of FIFO memory controller chips (see, e.g., FIGS. 9A-9B). As will be understood by those skilled in the art, a commonly accepted definition for the term "cascade" in the electrical arts is: "a series of components or networks, the output of each serving as the input for the next." (American Heritage College Dictionary, 3rd edition, © 1997). Accordingly, it cannot be reasonably maintained that FIG. 30 of document D1 discloses or suggests any cascaded arrangement of FIFOs that supports any standard mode of operation.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on February 9, 2005.

Candi L. Riggs

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Date of Signature: February 9, 2005